REMARKS

Claims 1-36 are pending. In the Office Action dated June 29, 2006, the Examiner rejected claims 1-36 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,587,912 to Leddige et al.

The disclosed embodiments of the invention will now be discussed in comparison to the applied references. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the subject matter described in the applied references, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

As the operating speed of processor-based systems continues to increase, it has become more important to precisely control the timing at which signals are transferred between different components of such systems. For example, processor-based systems using memory modules containing a memory hub coupled to a plurality of memory devices operate at a very high rate of speed. In such systems it can be difficult to coordinate the coupling of read data from the memory devices to the memory hub and from the memory hub to other components in the processor-based system. The disclosed memory hub solves this problem by including, *inter alia*, a read synchronization module that is coupled to the memory devices. The read synchronization module compares the timing between when read data are coupled from the memory devices, generally responsive to a read data strobe signal, and the timing when the read data are coupled from the memory hub, which is generally in synchronism with a core clock signal. Based on this comparison, the disclosed read synchronization module generates an adjust signal. The adjust signal is applied to a memory sequencer, which couples memory requests to the memory devices responsive to received memory requests. The memory sequencer uses the adjust signal to adjust the timing at which read memory requests are coupled to the memory devices. As a result, the memory sequencer can control the timing at which the read data are coupled from the memory devices to the memory hub. In this way, the timing at which the read data and read data strobe signal are coupled from the memory device to the memory hub can be

synchronized to a core clock signal that is used to clock the read data from the memory hub to another component in a processor-based system, such as a memory hub controller.

The sole reference cited in the Office Action is the patent to Leddige *et al.*, which discloses a memory system having a plurality of memory modules. Each of the memory modules includes several memory devices coupled to a memory repeater hub 520, which purportedly corresponds to applicant's memory hub. The memory repeater hub is shown in greater detail in Figure 7. According to the Office Action, the data handling logic 746 in the memory repeater hub 720 corresponds to applicant's read synchronization module. The entire description of the data handling logic 746 is found in column 8, lines 28-41, which reads as follows:

> The memory respector hub controller [*sic*] 720 further includes data handling logic 746 that may receive data from the data bus 727, reformat the data into a format appropriate for the memory devices on the memory module, and provides the reformated data to write buffer 712. The data may be stored in the write buffer 712 until the data is provided to a memory device the I/O circuitry 722. The data handling logic 746 may also receive data from the memory devices of the memory module via the data I/O circuitry 722 and/or read buffer 738. According to an embodiment of the present invention, the data handling logic 746 may be omitted and the formatting of data may be performed by the control logic 702.

Thus, the only function performed described by the data handling logic 746 is to reformat the data to a form that may be used by the memory devices connected to the memory repeater hub. The patent does not describe the data handling logic 746 as performing any of the functions of applicant's disclosed read synchronization module, including its function of comparing the timing between when read data are coupled from the memory devices and the timing when the read data are coupled from the memory hub. In fact, the patent does not describe the data handling logic 746 as performing *any* timing comparison function. Therefore, the disclosed data handling logic 746 does clearly does not suggest applicant's read synchronization module.

Not only does the Leddige *et al.* patent fail to disclose applicant's read synchronization module, but also fails to disclose applicant's memory sequencer or any other circuit that adjusts the timing at which read memory requests are coupled to memory devices. In fact, the Office Action does not even identify any component in the memory repeater hub 720 shown in Figure 7 that purportedly corresponds to applicant's memory sequencer. Instead, the Office Action contends the entire memory hub controller 720 corresponds to the memory sequencer. However, insofar as the disclosed data handling logic 746 does not provide an adjust signal indicative of the timing of read data being coupled from the memory devices compared to the timing of read data coupled from the memory hub, it certainly does not disclose the use of such adjust signal to control the timing at which read memory requests are coupled to memory devices.

Turning, now, to the claims, claim 1 is directed to a memory module having a plurality of memory devices and a memory hub. The memory hub includes, *inter alia*, a read synchronization module operable to compare timing between coupling read data from the memory devices and coupling read data from the memory hub and to generate an adjust signal corresponding thereto. As explained above, the disclosed data handling logic 746, which purportedly corresponds to applicant's read synchronization module, performs only a data formatting function; it does not perform any timing comparison function. The memory hub of claim 1 further includes a memory sequencer operable to the couple memory requests to the memory device interface and to adjust the timing at which such requests are coupled responsive to the adjust signal generated by the read synchronization module. As also explained above, the patent to Leddige *et al.* does not disclose any circuitry performing the function of altering the timing at which read requests are coupled to a memory device responsive to a signal indicative of any timing comparison. Claim 1 is therefore novel over the Leddige *et al.* patent.

The memory module of claim 1 is claimed in the context of a computer system in claim 20, and is therefore novel for the same reason that claim 1 is novel and because of the additional limitations added by claim 20.

Claim 8 is directed to a memory module including a plurality of memory devices and a memory hub. The memory hub includes, *inter alia*, a read synchronization module operable to compare timing between read data strobe signals and a core clock signal and to

generate an adjust signal corresponding to the compared timing. As explained above, the data handling logic 746 disclosed in the Leddige *et al.* patent does not perform this function, but instead performs only a data formatting function. The memory hub of claim 8 further includes a memory sequencer operable to couple memory requests to a memory device interface at times that are adjusted responsive to the adjust signal generated by the read synchronization module. As explained above, the Leddige *et al.* patent does not disclose this memory sequencer or any other circuitry performing the function of the claimed memory sequencer.

Claim 13 is directed to the memory hub that is included in the memory module of claim 1 and is therefore novel over the Leddige *et al.* patent for the same reason that claim 1 is novel.

Claim 27 is directed to a method of reading data from a memory module. The claim specifies, among other things, comparing timing between receiving read data and outputting the read data from a memory module. As explained above, the patent to Leddige *et al.* does not disclose any circuitry that performs this function. Claim 27 further specifies adjusting the timing at which read memory requests are coupled to the memory device interface as a function of the compare timing. Again, nothing in the system disclosed in the Leddige *et al.* patent performs this function. Claim 27 is therefore novel over the Leddige *et al.* patent.

Claim 33 is directed to a method of coupling read data from a memory device to a buffer and outputting read data from the buffer. The claim specifies that read data received responsive to read memory requests are stored in a buffer and subsequently output from the buffer. The timing between storing the read data in the buffer and outputting the read data from the buffer is compared, and this comparison is used to adjust the timing at which read memory requests are coupled to the memory device interface. Clearly the system disclosed in the Leddige *et al.* patent does not perform this function, and it therefore does not anticipate claim 33.

The claims dependent on the above-discussed independent claims are also novel over the Leddige *et al.* patent because of their dependency on novel independent claims and because of the additional limitations added by those claims.

All of the claims in the application. *i.e.*, claims 1-36, are clearly allowable. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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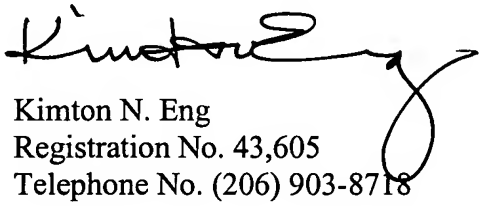

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